ABSTRACT OF THE DISCLOSURE

A method of making an isolation-less, contact-less array of bi-directional read/program non-volatile memory cells is disclosed. Each memory cell has two stacked gate floating gate transistors, with a switch transistor there between. The source/drain lines of the cells and the control gate lines of the stacked gate floating gate transistors in the same column are connected together. The gate of the switch transistors in the same row are connected together. Spaced apart trenches are formed in a substrate in a first direction. Floating gates are formed in the trenches, along the side wall of the trenches. A buried source/bit line is formed at the bottom of each trench. A control gate common to both floating gates is also formed in each trench insulated from the floating gates, capacitively coupled thereto, and insulated from the buried source/bit line. Transistor gates parallel to one another are formed in a second direction, substantially perpendicular to the first direction on the planar surface of the substrate. In one embodiment, openings between the rows of transistor gates are used to cut the floating gates in the trenches, without cutting the control gates.